

General Description

The XGMII is part of the IEEE802.3 standard that addresses 10GbE applications. XGMII provides a standard interface between the MAC and an external PHY, allowing for multiple PHY variations. It serves as an alternative to the 10 Gigabit Attachment Unit Interface (XAUI) or 10 Gigabit Sixteen-Bit Interface (XSBI). Several Physical Coding Sublayers (PCS/MAC) known as 10GBASE-X, 10GBASE-R and 10GBASE-W are also governed by the IEEE802.3 standard and are provided through 3rd party vendors as soft or hardened blocks for seamless implementation of the standard.

The implementation of the interface within the Rapid Bridge Platform provides the design flexibility to adopt different interfaces. The XGMII interface is available for use with HSTL and SSTL2 IO pads. Although the interface is targeted at IEEE802.3, it may be operated at higher frequencies at up to 312.5MHz or 625Mbps.

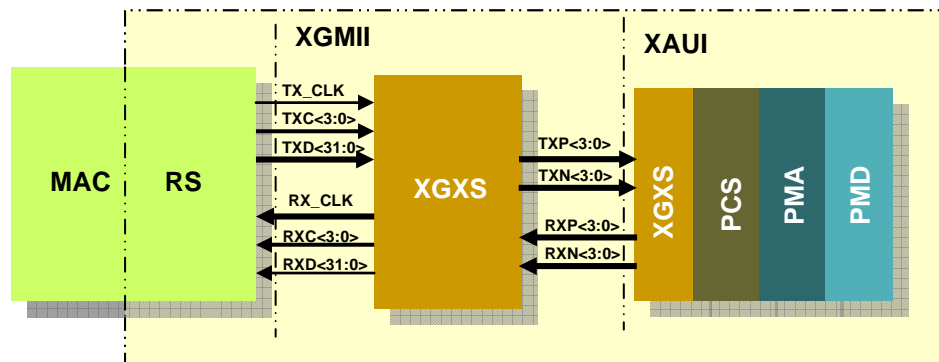


Figure 1: XGMII subsystem

XGMII Subsystem Overview

The XGMII subsystem acts as the interface between an external PHY and the PCS(MAC) layers. The subsystem is divided into transmitter and receiver blocks. The transmitter block receives 64 bits of data, 8 control signals, and a respective transmit clock from the MAC layer. It performs serialization and phase offsetting to transmit 32 bits of data, 4 bits of control signals and a 90° phase offset clock. The resulting data and control signals operate in double data rate mode and are eye-centered at 156.25MHz. The receiver block receives 32 bits of data, 4 bits of control signals, and a respective clock from the PHY layer. The data and control signals are captured using both edges of the clock and de-serialized. 64 bits of data, 4 bits of control signals and the respective clock are passed on to the MAC layer at single-data rate. The 32 bit data path is divided into four 8-bit lanes, with one control bit for each lane. The XGMII interface uses embedded delimiters rather than discrete signals. Should the control signal be asserted, delimiter or special characters are present on the respective lanes. When a control bit is de-asserted, the corresponding data path contains normal data characters. Delimiters and special characters are defined in the IEEE802.3ae document and include Idle, Start, Terminate and Error. Frame or packed sizes are constrained by the minFrameSize and maxFrameSize and are stripped on a per lane basis by the MAC(PCS) layer. Two versions of the subsystem are available to the end user, `sys_xgmii_X` and `sys_xgmii_id_X`.

The XGMII specification states that the clock and data on both transmit and receive sides are edge synchronized and additional delay must be inserted at the board level to accommodate the setup and hold time requirements. However, in the Rapid Bridge solution, both designs have the transmit clock eye-centered at the transmitter IOs. This eliminates the need for additional delay insertion in the clock path at the board level. In the `sys_xgmii_X` subsystem, the P_RXC clock is received by the receiver side eye centered and no internal manipulation is performed to provide adequate setup and hold margins. It assumes the phase offset for eye centering is generated at the board level or the PHY. In the `sys_xgmii_id_X` subsystem, an internal Master and Slave DLL are used to establish the necessary delay required by the receiver to sample the data. In this case, data and control signals are received edge aligned to the clock (no board delay is needed).

Transmit and receive clock may differ in operating frequency by ± 100 ppm. The MAC layer compensates for transmitter and receiver frequency offset. The `sys_xgmii_id_X` subsystem may be operated at frequency ranges of up to 312.5MHz. This is equivalent to double the data rate required by the 10GbE specification. The `sys_xgmii_X` may also be operated at the higher data rates. In general, the maximum data rate is limited by the board level matching of the traces and time of flight, mainly the controlled delay of the P_RXC to ensure adequate set up and hold margins.

Subsystem Pin Definition

Table 1 defines the signal pins for sys_xgmii_X and sys_xgmii_id_X subsystems.

Table 1: XGMII Subsystem Pin Definition

Symbol	Type	Interface	Function
P_TXC	Output	PHY	Transmit Clock: P_TXC is the transmit clock output to the PHY. P_TXC operates at 156.25MHz \pm 100ppm. P_TXC is phase delayed by 90° from P_TD and P_TX_CTL. This allows for accurate eye-centering of the transmit data.
P_TD<31:0>	Output	PHY	Transmit Data: Contains bits <15:0> and <31:16> on the rising and falling edges of P_TXC, respectively.
P_TX_CTL<3:0>	Output	PHY	Transmit Control Signal: Transmitted on both edges of the clock. Each bit corresponds to 8 bits of data (one per Lane). De-asserted during normal data transmission. Asserted during delimiter and special character transmission.
P_RXC	Input	PHY	Receive Clock: P_RXC is the received clock. Receive data is captured on the rising and falling edges of P_RXC.
P_RD<31:0>	Input	PHY	Receive Data: Bits <15:0> and <31:16> are captured on the rising and falling edges of P_RXC, respectively.
P_RX_CTL<3:0>	Input	PHY	Receive Control Signal: Sampled on both edges of P_RXC. Each bit corresponds to 8 bits of data (one per Lane). De-asserted during normal data transmission. Asserted during delimiter and special character transmission.
TX_CLKI	Input	Core	Internal Transmit Clock: Generated by crbp_interface_A, is a 156.25MHz clock used by the MAC and the subsystem.
TX_CLKQ	Input	Core	Internal Transmit Clock: Generated by crbp_interface_A, is the 90° phase delayed version of the internal clock used by the subsystem.
TD<63:0>	Input	MAC	Transmit Input: Transmit data is captured by the falling edge of TX_CLKI. Then it is serialized and synchronized to TX_CLKQ. Low bits <31:0> transmitted on rising edge, high bits <63:32> on fall.
TX_CTL<7:0>	Input	MAC	Transmit Enable: Control signals are captured by the falling edge of TX_CLKI and serialized using both edges of TX_CLKQ.
RXC	Output	MAC	Internal Receiver Clock: The internal version of the received clock, P_RXC used to capture and resynchronize receiver data.
RD<63:0>	Output	MAC	Receiver Output: De-serialized receiver data, synchronized to rising edge of RXC.
RX_CTL<7:0>	Output	MAC	Receiver Control signals: De-serialized receiver control signals, synchronized to rising edge of RXC.

sys_xgmii_X and sys_xgmii_id_X Implementation

The XGMII specification requires the data and control signals to be eye-centered at the receiving end. This may be achieved by additional trace length in the clock paths at the board level, or by compensating for the delay within the die. Two versions of the XGMII subsystem, sys_xgmii_X and sys_xgmii_id_X are provided to

meet end user's system requirements. Both subsystems incorporate a 90° phase offset internal clock based on a 156.25MHz operating frequency in the P_TXC path to establish the necessary 1.6ns delay. The `sys_xgmii_id_X` version also incorporates an additional `crb` template site that is configured as a Master DLL. Furthermore, one of the VSSC pad sites, `prbv_vssc`, is converted to a Slave DLL (`prba_dll_slave_A`). The Master DLL calculates a 7-bit digital code corresponding to 90° phase offset and the Slave DLL converts the 7-bit code to a delay element of 1.6ns that is placed in the P_RXC path to achieve the internal delay requirements. The end user has the option of using the `sys_xgmii_X` and adding the 1.6ns delay at the board level to the P_RXC path or configuring one of the `crb` templates to the Master DLL, instantiating `sys_xgmii_id_X`, and matching the data, control signals, and clock paths. In both cases, the 1.6ns delay in the P_TXC path is automatically added on the die, so no additional board delay is required. If the board is designed using FR4 material, trace delay is approximately 192ps/inch. Therefore the P_RXC path in the `sys_xgmii_X` implementation requires approximately an additional 8.5 inches of trace. Board designers should use a delay calculator to get exact numbers for the dielectric in their particular PCB.

Multiple Subsystem Configurations

Different versions of the XGMII subsystem with specific interface signaling levels are available for interfacing with different PHYs. The interface subsystems are listed in Table 2.

Table 2: Available XGMII subsystems

Subsystem	Description
<code>sys_xgmii_SSTL2</code>	Standard XGMII with SSTL2_Classi interface, 2.5V signaling levels
<code>sys_xgmii_HSTL</code>	Standard XGMII with HSTL_Classi interface, 1.5/1.8V signaling levels
<code>sys_xgmii_id_SSTL2</code>	XGMII with internally delayed receive clock and SSTL2_Classi interface , 2.5V signaling levels
<code>sys_xgmii_id_HSTL</code>	XGMII with internally delayed receive clock and HSTL_Classi interface , 1.5/1.8V signaling levels

10GbE MAC Layer

The Physical Coding Sublayers (PCS/MAC) 10GBASE-X, 10GBASE-R and 10GBASE-W, are provided through partnership with GDA technologies. They are compatible with the XGMII interface block. The MAC layer may be obtained in soft or hardened (place and routed) forms. Interoperability test benches and subsystem models are available for top level simulations.