Graphics Double Data Rate III (GDDRIII) IO

General Description

GDDRIII (Graphics Double Data Rate) is a 1.8V supply referenced IO buffer interface designed in accordance with ATI's GDDRIII x32 DRAM specification. The specified operating frequency for GDDRIII is 450, 500, 550 and 600MHz, for different configurations. However, the GDDRIII interface and the complete GDDRIII physical layer will operate up to 800MHz (1.6Gpbs) with proper link budgeting.

Rapid Bridge provides a complete memory solution that allows for operations in excess of 1.6Gbps. Consult the Double Data Rate Supplement for details.

Pad Set Definition

Table 1 contains the GDDRIII pad set definition.

Table 1: GDDRIII pad set definition

Name	Definition
prbs_gddriii_bidi	*Bi-directional single ended pad for all applications*

(1)For additional information on the functionality of these pads, see the Rapid Bridge Double Data Rate Supplement.
Other pads necessary for the operation of the GDDRIII can be found in the Rapid Bridge Support Pads Datasheet.

Table 2 defines the pins for the GDDRIII bidirectional IO pad.

Table 2: prbs_gddriii_bidi Pin Definition

Name	Definition	Type
PAD	*IO Pad, 1.8V signaling levels*	*Inout*
DOUT	*Output driver input*	*Input*
OE	*Output enable*	*Input*
TESTN	*Test enable, low speed/low power, for board level test*	*Input*
IE	*Input enable, powers down input receiver*	*Input*
DIN	*Receiver output, positive polarity*	*Output*
ODT<2:0>	*Enables 60/120/240 Ω termination to VDDQ when READ is asserted,* 000*:No termination,* 001*: 60Ω termination,* 010*: 120Ω termination,* 100*: 240Ω termination. Other combinations are illegal and will result in erroneous behavior.*	*Input*
READ	*Enables receiver termination*	*Input*
PI	*Nand input, used for board level continuity test*	*Input*
PO	*Nand output, used for board level continuity test*	*Output*
MODE_1_TEST	*JTAG test pin. When enabled (high), DOUT_TEST is routed to the normal DOUT path (PAD), and OE_TEST goes to OE.*	*Input*
DOUT_TEST	*JTAG test pin. Desired PAD output during test.*	*Input*
OE_TEST	*JTAG test pin. Desired OE state during test.*	*Input*
DIN_TEST	*JTAG test pin. Reflects DIN (PAD) during test.*	*Output*

MODEL SUPPORT

Models are provided to support the design, verification and validation in a standard COT flow allowing end users to take full advantage of latest tools and methodologies. Timing information

and constraints are embedded in the synthesis models for design and timing validation. Verilog models contain detailed functional and timing models and should be used to design the surrounding logical blocks. These models are not back-annotated from SDF or stuffed with dummy numbers, but have the actual Spice result integrated for proper timing performance. The models are constructed from gate level netlist and are complemented with behavioral models for the analog sections. The liberty models also contain the actual delay element timing, and may serve to address delay calculations. Refer to the list of supported models below:

- Liberty (.lib/.slib/.sdb/.db)
- Verilog
- LEF
- CEL, FRAM
- CLF
- TLF4.3
- GDSII
- CDL