

Common Mode Logic (CML) IO Cell

v1.2

Features / Benefits

- Output amplitude programmability for link/power optimization: 8/10/13/16mA steering currents
- Multiple Pre-emphasis programmability for link optimization: 2/4/8mA Pre-emphasis currents
- Up to 1.8GHz/3.6Gbps data rate
- Calibrated internal impedances
- 1.8V VDDQ supply voltage
- AC / DC Coupled
- Termination disable for Multi-drop applications
- Bi-directional
- IDDQ and parametric Nand test functions
- Less than $\pm 3\%$ duty cycle distortion across PVT
- Metal programmable within Rapid Bridge platform
- ESD 2kV HBM, 200V MM, 500V CDM
- Wirebond, Flip Chip and CUP versions available
- IEEE 1149.1 Compliant

Applications

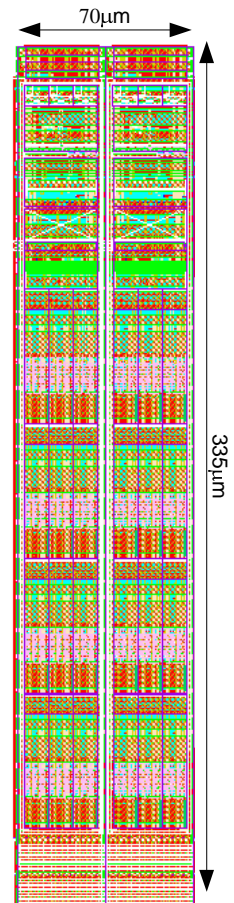
- High Speed interfaces up to 3.6Gbps
- Networking, Ramlink, Telecommunication
- Backplane connectivity
- High speed interface signaling
- ColIBlitz

Product Description

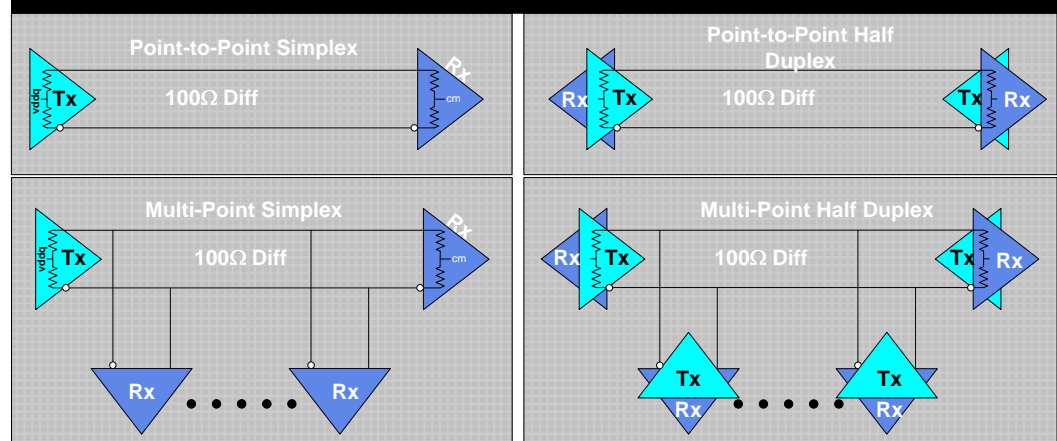
CML is based on Low Voltage Differential Signaling that results in minimum power dissipation and adequate noise margin, while enabling operating frequencies up to 1.8GHz. CML interface provides users with the highest operating frequency available within the platform. CML interface is primarily intended for point-to-point applications that require high speed signaling. Bi-directional and tri-state options are provided to allow for multi-drop applications at lower speeds in order to broaden the usage of the interface for proprietary applications. Output amplitude programmability allows for power/noise margin tradeoffs, while the programmable pre-emphasis levels allow for Inter Symbol Interference (ISI) compensation.

An SoC Approach

LiquidIO is integrated along with LiquidMXS and LiquidCell to create highly integrated, efficient and comprehensive LiquidPHY subsystems. The readily integrated subsystems addresses many challenges and concerns associated with high speed interface designs. CML IO is used in implementation of CoolBlitz PHY.



EXAMPLE APPLICATIONS OF CML





Common Mode Logic (CML) IO Cell

Complete Interface Solution

CML interface is part of a complete IO ring solution, which has been specifically designed for high performance, easy chip integration, and flexible system level requirements. This top-level integrated IO design approach eliminates redundant components, such as multiple bias generation and calibration circuits, and prevents power supply fragmentation, leading to smaller area, lower power utilization, and better ESD protection.

Because IOs are designed to work together, test methodology has been greatly simplified as well. Parametric Nand trees, JTAG scan chains, and IDDQ testing can all be accomplished with minimal circuits and control lines.

Proprietary software available from Rapid Bridge may be used to help create correct-by-construction IO rings with mixed IO types and the proper number of support pads for a successful design. IOCalculator software is a WEB based tool that allows end users to calculate power pad requirements based on packaging and system specifications for the supported standard within the Rapid Bridge LiquidIO family. RingComposer is used to compose the entire ring and the respective support circuits based on output of the IOCalculator. Test functions are composed and are correct by construction. The system level ESD results in better than 2kV HBM, 200V MM and 500V CDM models. Combination of above tool sets and metal programmability creates a complete liquid infrastructure allowing full flexibility and re-programmability.

For More Information...

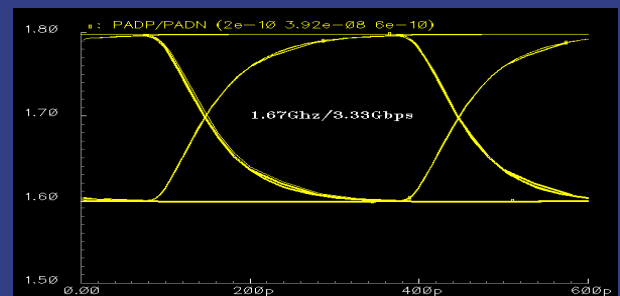
Regarding LiquidIP™, LiquidASIC™, or LiquidSoC™, please contact Rapid Bridge at:

sales-support@rapidbridge.com or visit www.rapidbridge.com

Performance Beyond the Past

CML is part of a harmonious system that is calibrated through a Central Calibration Unit across process and temperature. This yields significant improvement in rms and peak currents of up to 60%, reducing top level system requirements. Reduction in power is coupled with well matched and balanced output impedances that enhances signaling and performance throughout the system. Systematic implementation of LiquidIO subsystem eliminates potential, difficult to address, interface interactions.

CML 50Ω CM terminated, 1pf loa, no PE



CML 50Ω CM terminated, 1pf load, with 8mA Pre-emphasis

